UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/996,279	11/28/2001	Lothar Risch	L&L-I0178	4049

7590 09/24/2003

LERNER AND GREENBERG, P.A.
Post Office Box 2480
Hollywood, FL 33022-2480

EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 09/24/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/996,279	RISCH ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cov r sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 July 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 December 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Response to Amendment

Applicants' amendment filed on June 06, 2003 has been entered on July 09, 2003 and the request for an RCE filed on June 27, 2003 has been entered on July 09, 2003.

Therefore claim 1 as amended by the amendment of June 06, 2003 and claims 2-9 and 11 –19 as recited in the amendment of June 06, 2003 are currently pending in the application.

Election/Restrictions

Applicant's election without traverse of claims 1-20 in Paper No. 10 is acknowledged.

Applicants' cancellation of claims 21-25 is acknowledged.

Claim Rejections - 35 USC § 112

Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. (For response to Applicants' arguments see section below).

While applicant may be his or her own lexicographer, a term in a claim may not be given a meaning repugnant to the usual meaning of that term. See *In re Hill*, 161 F.2d 367, 73 USPQ 482 (CCPA 1947). The term "spacer layer " in claim 1 is used by the claim to mean " separation/filler" while the accepted meaning is "sidewall spacer".

It is suggested that Applicants' use the term " separation" instead of the recited "spacer".

Applicants' respond by stating, " spacer layer has been traditionally used to encompass the meaning of separating layer " and "that terms given the meaning separating layers can be found in claims of thousands of U.S. patents."

Applicants' have not provided a single patent to support their conclusion. Further it is well known in the semiconductor art (where the instant application belongs) that separating layer and spacer layer are two different things. A spacer layer is generally understood to mean a layer on the sidewalls of a gate and a separation layer is generally understood to mean a layer that separates two other elements.

The 112 rejection is made Final.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-2, 4-20 rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. (U.S. Patent No. 6,365,465, herein after Chang). Previously applied and in view of Burghartz et al. (U.S. Patent No. 5,461,250, herein after Burghartz) both previously Applied . (for response to Applicants' arguments see section below).

With respect to claim 1, Chang discloses a method of fabricating a double gate MOSFET, including the steps in the following sequence :

Providing a substrate having a silicon substrate layer (Fig. 1 A # 4, col. 4 lines 5-6); a first insulation layer disposed on the silicon substrate layer (Fig. 1 A # 3, col. 4 line 7); a first spacer layer disposed on the first insulation layer (Fig. 1 A #11); and a semiconductor layer disposed on the first spacer layer (fig. 1 A # 5): patterning the semiconductor layer resulting in a semiconductor layer structure provided as a channel of the double gate MOSFET (fig. 1 A #5, channel between s/d 9); depositing a second spacer layer on the semiconductor layer and the first spacer layer (fig. 3 A # 2);

It is noted that the newly added limitation " in the following sequence" it is noted that :

"Generally , Applicants' reversed order of process sequence as compared to the applied references including Chan , can not be considered as an act of invention, since reversing the order of prior art process step is held to render prima facie Obvious"

Ex Parte Rubin, 126 USPQ 440 (BAPI, 1959).

Further , " As a matter of fact selection of any order of performing process steps is prima fcie obvious in absence of new or unexpected results. "

In re Burhaus, 154 F.2d. 690, 69 USPQ 330 (CCPA 1946).

Therefore the sequence of performing the steps does not patentably distinguish the presently recited claim over the applied prior art.

Chang does not specifically disclose the step of completely embedding the semiconductor structure in the first and second spacer layers by patterning the first and second spacer layers.

However, Burghartz in figures1, 2 and col. 6 lines 4 to7 describe completely embedding the semiconductor structure in the first and second spacer layers by patterning the first and second spacer layers to decrease interface scattering and providing a region of high mobility charge carriers as near the gate as possible to maximize the capacitance and enhance device performance.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to include Burkhart's step of completely embedding the semiconductor structure in the first and second spacer layers by patterning the first and second spacer layers in Chang's method to decrease interface scattering and providing a region of high mobility charge carriers as near the gate as possible to maximize the capacitance and enhance device performance. (Burghartz col. 2 lines 60-65).

The remaining limitations of claim 1 are:

depositing a second insulation layer on the structure formed of the first and second spacer layers (fig. 3A # 7): vertically etching two depressions disposed along one direction, the two depressions dimensioned such that the semiconductor layer structure is situated completely between them: during the etching of the two depressions, the second insulation layer, the first and second spacer layers and, in each case on both sides, an edge section of the semiconductor layer structure being etched through completely in each case; filling the depressions with electrically conductive material (fig. 3 C # 17), forming a contact hole in the second insulation layer (Fig. 2Y # 11); selectively removing the first and second spacer layers through the contact hole made in the second insulation layer (fig. 1 D); applying a third insulation

layers on inner walls of a region of removed spacer layers and on surfaces of the semiconductor layer structure (figs. 20 to 2Q) and introducing a further electrically conductive material into the region of the removed spacer layers. (2Y # 12).

With respect to claim 2, wherein the substrate structure is formed by applying the first insulation layer, the first spacer layer, and the semiconductor layer one after another. (See claim1 above. It is noted that current case law is , "As a matter of fact selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results. In re Burhaus, 154 F.2d 690, 69 USPQ330 (CCPA 1946, therefore without a showing of criticality or unexpected results the recited order of steps is prima facie obvious).

With respect to claim 4, wherein the forming the substrate includes the steps of : Providing the silicon substrate functioning as a first semiconductor substrate (fig. 1A # 4); applying the first insulation layer on the first semiconductor substrate (Fig. 1 A # 3, col. 4 line 7); providing a second semiconductor substrate (Fig. 1 a # 12); applying the first spacer layer on the second semiconductor substrate (fig. 1A # 11); connecting the first and second semiconductor substrates to one another using a wafer bonding process between the insulation layer and the first spacer layer(Figs. 2A to 2C, col. 4 lines 46-61) and reducing a thickness of the second semiconductor substrate resulting in the semiconductor layer (col. 4 lines 58-60, boron etch).

With respect to claim 5, wherein the first and second spacer layers are formed from silicon nitride (fig. 2 F layers # 2 & 7).

With respect to claim 6, wherein the second insulating layer is planarized after being deposited.(fig. 2G and col. 6 lines 64-66).

With respect to claim 7, wherein the step of selectively removing the first and second spacer layers through the contact hole made in the second insulation layer.(fig. 2G).

With respect to claims 8 and 13, wherein the electrically conductive material is formed from a material selected from the group consisting of doped polycrystalline silicon, metal and silicide. (col. 6 lines 15-18).

With respect to claims 9 and 14, wherein the doped polycrystalline silicon is formed by Chemical Vapor phase deposition and a doping is performed during deposition. (col. 4 lines 27-29).

With respect to claim 10, the method comprises " selectively removing the first and second spacer layers by wet-chemical etching .(col. 6 lines 1-5).

With respect to claim 11, the method comprises applying the third insulation layers using a thermal oxidation process. (col. 6 line 10).

With respect to claim 12, wherein the step of producing a relatively thin oxide layer on the surface of the semiconductor layer structure and producing a relatively thick oxide layer on the inner walls of the region of the removed spacer layers. (figs. 2C and 2 T , col. 4 lines 47-49 and col. 6 lines 9-14).

With respect to claim 15, wherein an oxide layer is applied as the first insulation layer (fig. 1 A).

With respect to claim 16, wherein a silicon layer is applied as the semiconductor layer(col. 6 line 15-17).

With respect to claim 17, wherein an oxide is deposited as the second insulation layer. (fig. 2G).

With respect to claim 18, wherein an oxide layer is applied as the third insulation layer.(fig. 2G).

With respect to claim 19, wherein arsenic atoms are used in the doping process. (col. 7 line 43)

With respect to claim 20, wherein phosphorous atoms are used in the doping process.(col. 7 line 44).

B. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chan et al. (U.S. Patent No. 6,365,465, herein after Chan) as applied to claims 1-2 above, and further in view of Shimizu (U.S. Patent No. 5,753,541, herein after Shimizu).

With respect to claim 3, wherein the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

Chang does not specifically describe the step of recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam.

However, Shimizu, a patent from the same filed of endeavor, describes in col. 5 lines 33-38 describes the step of recrystallizing the semiconductor layer after being

applied by being irradiated with a laser beam to make the substrate a semi conductive layer.

It would have been obvious to one of ordinary skill in the art at the time of the invention to include Shimizu's laser annealing step(i.e. recrystallizing the semiconductor layer after being applied by being irradiated with a laser beam to make the substrate a semi conductive layer) in Chang's method so that further processing steps can use lower temperature than conventional methods wherein polycrystalline material is used. (Shimizu col. 3 lines 59-63).

Response to Arguments

Applicants' arguments with respect to claim 112 have been fully considered but not persuasive because Applicants' alleged supporting description e.g. Chan, Hu, Miyamoto all include description of channel separated from gate by " oxide film" or Gate oxide" film and not " spacer" as claimed by Applicants. Applicants' have not identified what the different uses and meanings of the term " spacer " in gambino and therefore a proper response cannot be given.

Applicant's arguments with respect to claims 1-25 have been fully considered but are not persuasive because as stated above the newly added limitation to the only independent claim 1 does not distinguish over the Applied prior art at least in view of current case law.

Applicants' contention that the Previous Office Action did not provide the motivation to combine the references is not entirely understood because the previous

O/A page 5 line 2 (Burhartz col. 2 lines 60-65) and page 8 lines 2nd last line Shimizu col. 3 lines 59-63) provides more than enough motivation to combine the references.

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (703) 306-5945. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7722.

Steven H. Rao

Patent Examiner

September 21, 2003.

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800